AMENDMENTS TO THE DRAWINGS

The attached sheets of drawings include changes to Figures 1, 2 and 4. In Figures 1, 2 and 4, the previously omitted legend --Prior Art-- has been added.

Attachment: Replacement Sheets for Figures 1, 2 and 4

REMARKS

Applicant respectfully requests further examination and reconsideration in view of the above amendments. Claims 1-10 remain pending in the case. Claims 1-10 are rejected. Claim 1 is amended herein. No new matter has been added.

DRAWINGS

Figures 1, 2 and 4 of the present Application are objected to because of the omission of the legend --Prior Art--. Enclosed herein are corrected Figures 1, 2 and 4. No new matter has been added.

SPECIFICATION

Applicant would like to thank Examiner for indicating that the abstract of the disclosure is longer than 150 words. The Applicant has made the appropriate correction herein of this informality.

CLAIM REJECTIONS - 35 U.S.C. § 112, second paragraph

Claims 1-10 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Specifically, Examiner rejects Claim 1 as being indefinite because Examiner asserts that the limitation "wherein said semiconductor die is disposed between said mounting surface

and said X-lead frame without bonding to said semiconductor die" does not clearly indicate what is not bonded to the semiconductor die.

Applicant has amended Claim 1 herein to recite the limitation "wherein said semiconductor die is disposed between said mounting surface and said X-lead frame without bonding to said mounting surface and without bonding to said X-lead frame." Applicant respectfully asserts that Claim 1 as amended clearly recites that the semiconductor die is not bonded to the mounting surface and is not bonded to the X-lead frame. Therefore, Applicant respectfully submits that Claim 1 overcomes the rejection under 35 U.S.C. § 112, second paragraph. Accordingly, Applicant respectfully submits that Claims 2-10 also overcome the rejection under 35 U.S.C. § 112, second paragraph, as these claims depend on Claim 1.

DOUBLE PATENTING REJECTION

Claims 1-10 are rejected under the judicially created (nonstatutory) doctrine of obviousness-type double patenting as being unpatentable over Claims 1-8 of U.S. Patent No. 6,747,342. A terminal disclaimer in compliance with 37 CFR §1.321 is being submitted concurrent with the instant response, thereby obviating the double patenting rejection.

CLAIM REJECTIONS - 35 U.S.C. § 103(a)

Claims 1 and 7-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over EU Patent Application Publication No. 370734 by Dunaway et al., hereinafter referred to as the "Dunaway" reference, in view of the Applicant Admitted Prior Art, hereinafter referred to as the "AAPA." Applicant has reviewed the cited references and respectfully submits that the present invention as recited in Claims 1 and 7-10 is patentable over the combination of Dunaway in view of the AAPA for the following rationale.

Applicant respectfully directs the Examiner to independent Claim 1 that recites that an embodiment of the present invention is directed to (emphasis added):

> A system mounting a semiconductor die within a package comprising:
> a mounting surface;
> an X-lead frame coupled to said mounting surface; and
> said semiconductor die, wherein said semiconductor die is disposed between said mounting surface and said X-lead frame without bonding to said mounting surface and without bonding to said X-lead frame.

Claims 7-10 that depend from independent Claim 1 provide further recitations of the features of the present invention.

Dunaway and the claimed invention are very different. Applicant understands Dunaway to teach a semiconductor chip package including a

bonding system for selectively connecting conductive elements of the package to pads of a semiconductor chip (Abstract). Dunaway teaches that the conductive elements include preformed solder bumps that can be bonded to the pads of the chip (col. 7, lines 24-30). In particular, Dunaway teaches that the preformed solder bumps are reflowed for bonding the leadframe conductive elements with the chip interface pads (col. 9, lines 4-6 and 12-19). With reference to Figure 7B of Dunaway, solderable conductive elements 70 of semiconductor wafer 72 are aligned with patterned solder bumps 16 on transfer surface 22. The patterned solder bumps 16 are heated and reflowed into wetted contact with conductive elements 70 (col. 11, lines 14-22). Specifically, solder bumps 16 are bonded to conductive elements 70.

In contrast, embodiments of the claimed invention are directed towards a system mounting a semiconductor die within a package including "wherein said semiconductor die is disposed between said mounting surface and said X-lead frame without bonding to said mounting surface and without bonding to said X-lead frame," as claimed (emphasis added). With reference to the present specification, the present invention describes that "[t]he X-lead frame is thus a structure providing electrical coupling between the drain region of the JFET die and an external lead in the absence of any bonding to the JFET die," "[e]lectrical coupling between the JFET source region and an external lead is thus provided in the absence of any bonding to the JFET die," and "[e]lectrical coupling between the JFET gate region and an external lead is thus provided in

the absence of any bonding to the JFET die" (emphasis added; page 7, line 22 through page 8, line 2; page 8, lines 11-13; and page 8, lines 22-23).

With reference to Figure 7 of the present specification, a cross-sectional view of power JFET die 720 disposed between mounting surface 710 and an overlying X-lead frame 735. JFET die 720 includes drain region 730 on the upper surface and source region 750 and gate region 760 on the lower surface. Now with reference to Figure 5 of the present specification, region 523 is shown for making mechanical and electrical contact with the source region of the JFET die without bonding to the JFET die (page 13, lines 4-8). Moreover, region 532 is shown for making mechanical and electrical contact with the gate region of the JFET die without bonding to the JFET die (page 13, lines 12-16). Furthermore, dashed line 540 indicate a position for placement of the JFET die between the mounting surface and an X-lead frame for providing mechanical support for the die as well as electrical coupling between the die and external leads without bonging to surface areas of the die (page 13, line 18 through page 14, line 2).

Applicant respectfully asserts that Dunaway in particular does not teach, disclose, or suggest "wherein said semiconductor die is disposed between said mounting surface and said X-lead frame without bonding to said mounting surface and without bonding to said X-lead frame," as claimed. In contrast, Dunaway discloses a semiconductor chip package including a bonding

system for reflowing and bonding conductive elements of the package to pads of a semiconductor chip. By teaching a system that bonds conductive elements of the package to pads of the semiconductor chip, Dunaway teaches away from the limitation "without bonding to said mounting surface and without bonding to said X-lead frame" of the claimed invention.

Furthermore, Applicant respectfully asserts that the combination of Dunaway and the AAPA fails to teach or suggest the claimed embodiments because the AAPA does not overcome the shortcomings of Dunaway. The AAPA, alone or in combination with Dunaway, does not show or suggest a system mounting a semiconductor die within a package including "wherein said semiconductor die is disposed between said mounting surface and said X-lead frame without bonding to said mounting surface and without bonding to said X-lead frame," as claimed (emphasis added).

Applicant respectfully asserts that nowhere does the combination of Dunaway in view of the AAPA teach, disclose or suggest the claimed embodiments of the present invention as recited in independent Claim 1, that this claim overcomes the rejection under 35 U.S.C. § 103(a), and is in a condition for allowance. Therefore, Applicant respectfully submits that the combination of Dunaway in view of the AAPA also does not teach, disclose or suggest the additional claimed features of the present invention as recited in Claims 7-10 that depend from independent Claim 1. Applicant respectfully

submits that Claims 7-10 also overcome the rejection under 35 U.S.C. § 103(a) as these claims are dependent on allowable base claims.

Claim 2 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Dunaway in view of the AAPA, further in view of United States Patent No. 5,293,058 by Tsividis, hereinafter referred to as the "Tsividis" reference. Claim 2 depends from independent Claim 1. Applicant has reviewed the cited references and respectfully submits that the present invention as recited in Claim 2 is patentable over the combination of Dunaway in view of the AAPA, further in view of Tsividis for the following rationale.

As described above, Applicant respectfully asserts that the combination of Dunaway in view of the AAPA, does not show or suggest a system mounting a semiconductor die within a package including "wherein said semiconductor die is disposed between said mounting surface and said X-lead frame without bonding to said mounting surface and without bonding to said X-lead frame," as claimed (emphasis added). In contrast, Dunaway discloses a semiconductor chip package including a bonding system for reflowing and bonding conductive elements of the package to pads of a semiconductor chip. By teaching a system that bonds conductive elements of the package to pads of the semiconductor chip, Dunaway teaches away from the limitation "without bonding to said mounting surface and without bonding to said X-lead frame" of the claimed invention.

Furthermore, Applicant respectfully asserts that the combination of Dunaway in view of the AAPA, further in view of Tsividis, fails to teach or suggest the claimed embodiments because Tsividis does not overcome the shortcomings of Dunaway in view of the AAPA. Applicant understands Tsividis to teach a linear voltage-controlled resistance element. Tsividis, alone or in combination with Dunaway in view of the AAPA, does not show or suggest a system mounting a semiconductor die within a package including "wherein said semiconductor die is disposed between said mounting surface and said X-lead frame without bonding to said mounting surface and without bonding to said X-lead frame," as claimed (emphasis added).

Applicant respectfully asserts that nowhere does the combination of Dunaway in view of the AAPA, further in view of Tsividis teach, disclose or suggest the claimed embodiments of the present invention as recited in independent Claim 1, that this claim overcomes the rejection under 35 U.S.C. § 103(a), and is in a condition for allowance. Therefore, Applicant respectfully submits that the combination of Dunaway in view of the AAPA, further in view of Tsividis also does not teach, disclose or suggest the additional claimed features of the present invention as recited in Claim 2 that depends from independent Claim 1. Applicant respectfully submits that Claim 2 also overcomes the rejection under 35 U.S.C. § 103(a) as this claim is dependent on allowable base claims.

Claims 1-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over United States Patent No. 6,040,626 by Cheah et al., hereinafter referred to as the "Cheah" reference, in view of United States Patent No. 6,809,408 by Yu et al., hereinafter referred to as the "Yu" reference. Applicant has reviewed the cited references and respectfully submits that the present invention as recited in Claims 1-10 is patentable over the combination of Cheah in view of Yu for the following rationale.

Cheah and the claimed invention are very different. Applicant understands Cheah to teach a semiconductor package where the semiconductor die is bonded to a plate portion (Abstract). With reference to Figure 6 of Cheah, a curable conductive material 46 is disposed between the lower surface of the plate portion 30 and the metalized region 18 of semiconductor die 16 such that plate 30 is firmly coupled to metalized region 18 (col. 3, lines 59-63; and col. 4, lines 30-50). Moreover, with reference to Figure 5 of Cheah, metalized region 19 defining a gate of die 16 is electrically coupled to terminal 12b via wire bond 20 (col. 4, lines 15-22). In particular, metalized regions 18 and 19 are bonded to plate 30 and terminal 12b, respectively, via a curable conductive material, such as solderable metal.

In contrast, embodiments of the claimed invention are directed towards a system mounting a semiconductor die within a package including "wherein

said semiconductor die is disposed between said mounting surface and said X-lead frame without bonding to said mounting surface and without bonding to said X-lead frame," as claimed (emphasis added). As described above, the present specification described that "[t]he X-lead frame is thus a structure providing electrical coupling between the drain region of the JFET die and an external lead in the absence of any bonding to the JFET die," "[e]lectrical coupling between the JFET source region and an external lead is thus provided in the absence of any bonding to the JFET die," and "[e]lectrical coupling between the JFET gate region and an external lead is thus provided in the absence of any bonding to the JFET die" (emphasis added; page 7, line 22 through page 8, line 2; page 8, lines 11-13; and page 8, lines 22-23). In particular, the JFET die is not bonded to the external leads.

Applicant respectfully asserts that Cheah in particular does not teach, disclose, or suggest "wherein said semiconductor die is disposed between said mounting surface and said X-lead frame without bonding to said mounting surface and without bonding to said X-lead frame," as claimed. In contrast, Cheah discloses a semiconductor package where the semiconductor die is bonded to electrical connectors. By teaching a system that bonds electrical connectors of the package to the semiconductor chip, Cheah teaches away from the limitation "without bonding to said mounting surface and without bonding to said X-lead frame" of the claimed invention.

Furthermore, Applicant respectfully asserts that the combination of Cheah and Yu fails to teach or suggest the claimed embodiments because Yu does not overcome the shortcomings of Cheah. Applicant understands Yu to teach a semiconductor package with a die pad having a recessed portion. In particular, Yu teaches that a chip is bonded to a die pad. With reference to Figure 2C of Yu a die bonding process is performed, wherein chip 11 is bonded to die pad 100 using adhesive 14. Moreover, Figure 2D of Yu teaches a wire bonding process for bonding chip 11 to lead frame 10 using gold wires 12.

Yu, alone or in combination with Cheah, does not show or suggest a system mounting a semiconductor die within a package including "wherein said semiconductor die is disposed between said mounting surface and said X-lead frame without bonding to said mounting surface and without bonding to said X-lead frame," as claimed (emphasis added). Moreover, by teaching a system that bonds a die to a chip, Yu teaches away from the limitation "without bonding to said mounting surface and without bonding to said X-lead frame" of the claimed invention.

Applicant respectfully asserts that nowhere does the combination of Cheah in view of Yu teach, disclose or suggest the claimed embodiments of the present invention as recited in independent Claim 1, that this claim overcomes the rejection under 35 U.S.C. § 103(a), and is in a condition for allowance. Therefore, Applicant respectfully submits that the combination of

Cheah in view of Yu also does not teach, disclose or suggest the additional claimed features of the present invention as recited in Claims 2-10 that depend from independent Claim 1. Applicant respectfully submits that Claims 2-10 also overcome the rejection under 35 U.S.C. § 103(a) as these claims are dependent on allowable base claims.

CONCLUSION

In light of the above remarks, Applicant respectfully requests reconsideration of the rejected claims. Based on the arguments presented above, Applicant respectfully asserts that Claims 1-10 overcome the rejections of record and, therefore, Applicant respectfully solicits allowance of these Claims.

The Examiner is invited to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,
WAGNER, MURABITO & HAO L.L.P.

Dated: 26 Oct, 2005

Matthew J. Blecher
Registration No. 46,558

Two North Market Street
Third Floor
San Jose, CA 95113
(408) 938-9060

APPENDIX

Attachment: Replacement Sheets for Figures 1, 2 and 4

Terminal Disclaimer